Model 560-5907/08 PCI-SG2

PCI Plug-In Card

Generator
Synchronized Generator
GPS Synchronized Generator

Serial Number_____

Rev. D
May 19, 2003

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Preface

Manual Organization

This manual contains the following chapters:

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Conventions

The conventions used in this manual are:

	=	Tips and clarifications.
 **WARNING**	=	Actions to prevent equipment damage.
Bold	=	Used to show messages, menu items, etc., that appear on a computer screen. For example, click on **Submit Changes**.
`text`	=	Used to indicate text you should enter with your keyboard, *exactly* as printed.
`text`	=	Used to display output character strings.

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Each new product manufactured by Symmetricom is warranted for defects in material or workmanship for a period of one year from date of shipment ("Limited Warranty"). Defects in material or workmanship found within that period will be replaced or repaired, at Symmetricom's option, without charge for material or labor, provided the customer returns the equipment, freight prepaid, to the Symmetricom factory under this limited warranty. Symmetricom will return the repaired equipment, freight prepaid, to the customer's facility. This one year Limited Warranty does not apply to any software or to any product not manufactured by Symmetricom.

If on-site warranty repair or replacement is required, the customer will be charged the then current field service rate for portal-to-portal travel time plus actual portal-to-portal travel charges. There is no charge for on-site warranty repair labor.

Products not manufactured by Symmetricom but included as integral part of a system (e.g. peripherals, options) are warranted for 90 days, or longer as provided by the original equipment manufacturer, from date of shipment.

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Proprietary Notice

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Introduction

1.1 General Information

This manual section will briefly describe the features of the GPS-PCI 2 and PCI-SG 2 cards. Sections 1.7, 1.10, 1.2.15, 1.2.19, 3.3.6, 3.3.15, 3.3.17, 3.3.18, and 3.5.4 are exclusively for the GPS model. All other sections apply to both models. References in the manual to the PCI card refer to both product models, which contain the same basic PCI card. These timing cards are not fully compliant with the PCI Local Bus Specification, Revision 2.1 or 2.2.

Model 560-5907 (PCI-SG 2) and 560-5908 (GPS-PCI 2) may be used in either Generator or Synchronized Generator mode, supplying precise time (100's nanoseconds through thousands of years) to the host computer. When the card is operating as a Synchronized Generator the output signals are synchronized to the timing reference. The PCI card phase locks to the timing reference and controls the on-board oscillator to remove frequency errors. If the timing reference is lost, the PCI card continues to increment time and output timing signals based upon the on-board oscillator's frequency (flywheeling).

The PCI card includes a real-time clock. This feature is an automatic no maintenance capacitor backup, which enables the PCI card to continue incrementing time in the event of a power failure. The capacitor powers the real-time clock for a minimum of 48 hours.

1.1.1 Mode Select

The PCI card operating modes that may be selected are as follows:

Generator Mode

Use this mode when an external reference is not used. In the Generator mode, the time may be started, stopped and preset via the PCI bus. In this mode, the Generator time accuracy is a function of the drift rate of the on-board oscillator.

Synchronized Generator Mode

The Model 560-5907 and 560-5908 cards may be synchronized by one of the following input references:

IRIG-B (AM)	Year entry required
IRIG-A (AM)	Year entry required
IRIG-B (DC)	Year entry required
IRIG-A (DC)	Year entry required
1 PPS	Complete time entry required

In the Synchronized Generator mode, the card is synchronized by an external reference. The on-board oscillator is disciplined to this input reference so that the card's drift rate is a function of the external reference.

GPS Mode (Model 560-5908 only)

The Model 560-5908 card may be synchronized by any of previously listed references or by GPS. This mode allows the Global Positioning System to automatically synchronize the PCI card to UTC time. The GPS Module assumes a moderate dynamic environment (LAND mode, velocity < 120 knots). The fix mode is AUTO 2-D/3-D and is preferable for most LAND applications.

1.1.2 Software Time Capture

When time is requested by software, the time from 100's of nanoseconds through thousands of years is captured when the request is received. The captured time is available to the host in packed BCD format and is independent of the Event Capture registers. The captured time will be compensated for local offset and daylight saving time if those settings have been made. The Software Time Capture Logic processes requests as fast as every 200 ns.

There is a maximum 150 ns delay from the time that a request is received until the time is ready.

1.1.3 Event Time Capture

The time from 100's of nanoseconds through thousands of years is captured when the specified edge (rising or falling) of the event signal occurs. The captured time is available to the host in packed BCD format. The Event Time Capture may be selected to trigger by one of the following signals:

- External Event
- PCI card Rate Generator
- PCI card Rate Synthesizer
- PCI card Time Compare

When an event occurs, the time is latched into the Event Time Registers and the Event Status Bit is set at location 0F8. If interrupts are enabled, a interrupt occurs concurrently with the status bit being set. Although the event capture can handle rates faster than most PC's can handle, the event hardware keeps only one time until the Event Status Clear Bit is set at 0F8.

1.1.4 Time Zone Adjustment

The Time Zone Offset Register is used to convert UTC time (either the time from the input reference or the generator) to Standard Time. The range of the time zone adjustment is from –12:59 to +12:59 hours.

1.1.5 Daylight Saving Time Adjustment

The card provides the ability to automatically handle DST transitions in any mode if DST is enabled. The transition takes place at 2:00 a.m. local time on the first Sunday in April and the last Sunday in October.

1.1.6 Leap Second

The PCI card will add an extra second at the end of the current UTC day if the Leap Second setting is made.

1.1.7 Phase Compensation (Cable Length Adjustment)

The PCI card has the ability to correct its timing outputs for phase delay caused by cabling. The range of compensation is from -800 to +800 µs with 100's of nanoseconds resolution. Positive adjustments moves the PCI Card outputs earlier in time. Negative adjustments move the PCI Card outputs later in time.

1.1.8 AM Timecode Output

The PCI card provides IRIG-B122 code as an output. The output may be selected to be on J1 "CODE OUT" BNC. The output voltage is factory set to 3 Vp-p into 600 ohms with a ratio of 3:1.

1.1.9 DC Timecode Output

The PCI card provides IRIG-B002 code as an RS-422 level output on the D9, pin 8 (+), pin 9 (–). The DC Timecode output may also be selected to be on J1 "CODE OUT" BNC.

1.1.10 Rate Generator Output

The Rate Generator outputs a signal at pin 7 of the D9 connector, output may also be selected on J1 "CODE OUT" BNC, with one of the following rates:

Disabled, 1 PPS, 10 PPS, 100 PPS, 1k PPS, 10k PPS, 100k PPS, 1 MPPS, 5 MPPS or 10 MPPS.

The Rate Generator signal is synchronous with the board timing and the rising edge is on time. With the exception of the 10 MPPS rate, the rate generator outputs have a 50% duty cycle. The 10 MPPS output is a function of the on-board oscillator's duty cycle (typically, 40-60%). The Rate Generator bit of the Hardware Status Register (location 0xFE) indicates when a Rate Generator rising edge has occurred

1.1.11 Rate Synthesizer Output

The Rate Synthesizer may be output on pin 6 of the D9 connector, which is selectable for either Time Compare or Rate Synthesizer output. The Time Compare may also be selected to be output on J1 “CODE OUT” BNC.

The Rate Synthesizer may be selected to output rates from 1 PPS to 1 MPPS in 1 PPS increments. The Output is a squarewave (50% duty cycle) and the edge may be selected to be either rising or falling on time. The Rate Synthesizer bit of the Hardware Status Register (location 0xFE) indicates when the rising edge (not on-time edge) of the Rate Synthesizer has occurred. A PCI interrupt is generated on occurrence of the rising edge, if enabled.

1.1.12 1 PPS Output

This PCI card output is on pin 5 of the D9 connector. The 1 PPS may also be selected to be on J1 “CODE OUT” BNC. This signal is rising edge on time and has a 50% duty cycle. A PCI interrupt is generated on occurrence of the rising edge, if enabled.

1.1.13 Time Compare Pulse Output

The Time Compare may be output on pin 6 of the D9 connector, which is selectable for either Time Compare or Rate Synthesizer output. The Time Compare may also be selected to be output on J1 “CODE OUT” BNC.

The Time Compare Output generates a 1 ms pulse that occurs when the Time Compare setting matches the PCI card’s time. Time Compare can be used to output pulses at regular time intervals. The Time Compare bit of the Hardware Status Register (location 0xFE) indicates when a Time Compare has occurred. A PCI interrupt is generated on occurrence of the rising edge, if enabled.

1.1.14 BNC Output Source Select

J1 “CODE OUT” BNC may be selected to output any of the following signals:

- IRIG-B AM (IRIG-B122)
- IRIG-B DC (IRIG-B002)
- Rate Generator
- Rate Synthesizer
- Time Compare
- 1 PPS

1.1.15 Antenna Position Setup (560-5908 only)

In GPS mode, the user’s position (longitude, latitude, and altitude) may be preset to speed satellite acquisition at turn on (refer to register, location 0x164 through 0x173).

1.1.16 Stored Configuration

Several parameters are retained in Electrically Erasable Programmable Read Only Memory (EEPROM) while the PCI card power is off. The following parameters define the configuration of the PCI card:

- Rate Generator Output
- Rate Synthesizer Output
- Phase Compensation
- Current Year
- Operating Mode
- Synchronized Generator Reference
- Daylight Savings Time Flag\Time Zone
- Time Compare Settings
- External Event Setup
- Time Quality Flag Useage

Both the Daylight Savings Time (DST) flag and Time Zone are saved, however, the Symmetricom driver resets both to 0 at start-up.

Note that the EEPROM has a finite number of write cycles (100,000).

1.1.17 Time Quality Flags

When operating in IRIG Synchronized Generator mode, the PCI card may be set to read the lock and four time quality status bits from a Symmetricom IRIG source. These five bits are encoded in the Control Field (P5) on various models of Symmetricom clocks. The status bits will allow the user of the PCI card to decide whether the IRIG source should be used for synchronization (see Section 3.3.8)

1.1.18 On Card Status LEDs

DS1 (top):

This LED blinks at a 1 PPS rate when the PCI-SG is in Synchronized Generator mode and has locked to the input reference. This LED is OFF when in Generator mode or when unlocked to the input reference in Synchronized Generator mode.

DS2 (middle):

This LED is ON when the Rate Synthesizer PLL is locked to the master 10 MHz on-board oscillator. This LED blinks at a 1 PPS rate when the PLL is unlocked. If the Rate Synthesizer is being used, contact service for assistance (if not used, ignore theLED).

DS3 (bottom):

This LED is ON at turn on and OFF when the FGPA has been successfully programmed.

1.1.19 12 Volt Antenna Feed (560-5908 only)

The Model 560-5908 supplies +12 VDC to the antenna BNC and will support Symmetricom's universal GPS antenna as well as the Down/Up converter.

WARNING

The GPS-PCI 2 card requires a +12 VDC antenna and may severely damage any antenna that does not support +12 VDC. For non-standard antenna types, contact Symmetricom for assistance. A connection to an older style +5 VDC antenna will destroy the antenna.

1.2 Physical Specifications

The PCI card is a single-slot PCI-compatible short card (6.875 in [17.463 cm] long).

1.3 Environmental Specifications

Operating Temperature:	0° to +50°C (+32° to +122°F)
Storage Temperature:	-17° to +100°C (0° to +212°F)
Humidity:	95% relative, non-condensing

1.4 Power Specifications

The PCI host computer powers the card.

Model 560-5907

+12 VDC @ 35 mA
- 12 VDC @ 20 mA
+ 5 VDC @ 150 mA

Model 560-5908 (GPS) with standard Antenna:

+12 VDC @ 70 mA
- 12 VDC @ 20 mA
+ 5 VDC @ 300 mA

1.5 Antenna Specifications (560-5908)

To operate in the GPS Synchronized Generator mode, the unit requires an external antenna. The standard antenna supplied with this option is part number 142-614-50, which includes 50 feet (15.24 meters) of coaxial cable. Cable lengths from 200 feet (60.96 meters) to 1,500 feet (457.2 meters) require the antenna Down/Up Converter option, part number 142-6150.

WARNING

Model 560-5908 supplies +12 VDC to the antenna BNC. Connection to an older +5 VDC antenna will destroy the antenna.

The general specifications for the 142-614-50 antenna are:

Size:	2.625 in diameter x 1.5 in (6.67 cm dia x 3.81 cm)
Weight:	0.55 lb. (0.250 kg) (including mounting mast)
Operating Temperature:	–40°C to +70°C (–40°F to +158°F)
Storage Temperature:	–55° to +85° C (–67°F to +185°F)
Humidity:	100% condensing
Power:	25 mA @ 12 V (supplied by card)

The cable specifications for the 142-614 antenna are:

Type:	RG-59
Length:	50 feet (15.24 meters)
Weight:	1.2 lb. (0.545 kg)
Humidity:	All weather, outdoors
Connectors:	TNC male to BNC male

If you have the optional 142-6150 Down/Up Converter antenna, please refer to its manual for specifications. Antenna and Down/Up Converter units are mounted on a 12-inch (30.48 cm) long PVC mast with 3/4-inch (1.9 cm) Male Pipe Thread (MPT) on both ends. The above specified weights include this mounting mast. Unless noted otherwise, increase the above specified sizes by approximately 11.25 inches (28.58 cm) to include the mounting mast.

1.6 Signal / Timing Specifications (560-5907 and 560-5908)

Amplitude-Modulated Reference Code Input

Format:	IRIG-B AM (amplitude-modulated) or IRIG-A AM (amplitude-modulated)
Amplitude:	0.5 to 10 Vp-p
Impedance:	Selectable, 10k, 600 Ω or 50 Ω to GND
Ratio:	2:1 to 5:1
Error Bypass:	3 frames
Phase Accuracy:	<3 µs with stable input reference
Phase Compensation:	±800 µs in 100 ns steps
Oscillator Tuning Range:	$5x10^{-6}$
Connector:	Rear-panel female BNC “CODE IN”

DC-shift Reference Code Input

Format:	DC-shift IRIG-B002 or
Format:	DC-shift IRIG-A002
Levels:	RS-422 or TTL
Impedance:	Jumper-Select: 120 Ω or HI (4 kΩ minimum)
Error Bypass:	3 frames
Phase Accuracy:	<1 µs with stable input reference
Connector:	Rear-panel D9 Pin 3 (+), 4 (–) for RS-422 levels Pin 3 (SIG), 2 (GND) for TTL levels

1.7 External Event / 1 PPS Reference Input

Active Edge External Event:	Selectable: Rising or Falling
Active Edge 1 PPS Reference:	Rising
Levels:	Logic 0: -0.5 to +1.75 VDC
	Logic 1: +2.25 to 5.0 VDC
Impedance:	Approximately 2 kΩ
Phase Accuracy (1 PPS):	<1 µs, typically <500 ns with stable input reference
Connector:	Rear panel D9 subminiature, pin 1

1.8 GPS Timing Specifications (560-5908)

Timing Accuracy:	< 1 µs to UTC
Position Accuracy:	Latitude, longitude, and elevation 25 meters SEP without SA
Acquisition Time:	20 minutes on cold start with power cycle, worst case scenario
Receiver Input:	Frequency: 1575.42 MHz (L1)
Code:	Coarse Acquisition (C/A)
Tracking:	8 satellites (4 for solution, 6 reported)
Connector:	Rear panel female BNC “ANTENNA” BNC supplies +12 VDC antenna power

1.9 Output Signal Specifications

1.9.1 Amplitude-modulated Generator Code Output

Format:	IRIG-B122
Amplitude:	Factory set for 3 Vp-p into 600 Ω to ground
Fixed Ratio:	3:1
Connector:	Selectable on rear-panel “CODE OUT” BNC

1.9.2 IRIG-B DC Generator Code Output

Format:	DC-Shift IRIG-B002
Levels:	RS-422 on D9, ACMOS on BNC
Connector:	Rear-panel D9 subminiature, pin 8 (+), pin 9 (–) or selectable on “CODE OUT” BNC

1.9.3 Time Compare Output

Resolution:	1 µs
Pulse Width:	1 ms
Compare Mask:	Milliseconds through hundreds of days
Levels:	ACMOS
Timing:	Rising edge on time
Connector:	Selectable or rear-panel D9 subminiature, pin 6; or selectable on “CODE OUT” BNC

1.9.4 1 PPS Output

Rate:	1 PPS
Duty Cycle:	50%
Amplitude:	ACMOS
Timing:	Rising edge on time
Connector:	Rear-panel D9 subminiature, pin 5; or selectable on “CODE OUT” BNC

1.9.5 Rate Generator Output

Timing:	Rising edge on time
Selectable Rates:	1 PPS, 10 PPS, 100 PPS, 1k PPS, 10k PPS, 100k PPS, 1 MPPS, 5 MPPS or 10 MPPS
Levels:	ACMOS

Connector:	Rear-panel D9 subminiature, pin 7; or selectable on "CODE OUT" BNC

1.9.6 Rate Synthesizer Output

Timing:	Selectable Rising or Falling on-time edge
Rates:	1 PPS to 1 MPPS in 1 PPS increments
Jitter:	30 ns
Levels:	ACMOS, squarewave
Connector:	Selectable on rear-panel D9 subminiature, pin 6; or selectable on "CODE OUT" BNC

1.10 General Specifications

SyncGen Timing Accuracy: <3 µs - IRIG-A or B (AM) modes

<1 µs - IRIG-A or B (DC) modes

<1 µs - 1 PPS mode

<1 µs to UTC-USNO - GPS mode (560-5908)

TCVCXO disciplined oscillator:

Frequency: 10.000 MHz

Frequency Stability (w/ref): $<1x10^{-7}$, typically $5x10^{-8}$

Aging: <1 PPM/Year

Leap Year: Automatically resets to day 1 after day 365 in standard years and after day 366 in leap years.

Leap Second: Automatically handles leap seconds in GPS mode (560-5908). User-programmable on day of occurrence in SyncGen mode.

Interrupts: Single PCI Interrupt

Lock Criteria:

IRIG AM Codes (A, B): One input on-time mark within 600 ns of the output on-timemark AND eight consecutive input on-time marks all of which are less than 1.5 µs from the output the aggregate error is less than eight µs.

IRIG DC Codes PPS, GPS: One input on-time mark within 300 ns of the output on-time mark AND eight consecutive on-time marks in which none have an error of greater than 500 ns.

Unlock Criteria:

IRIG AM Codes A, B: Five out of ten on time marks have an error of greater than three µs.

DC Codes PPS, GPS IRIG DC:

Five out of ten on time marks have an error of greater than one µs.

Lock Time:

Sync Gen (non-GPS): Minimum 15 seconds

Maximium two minutes

1.11 Factory Defaults

1.11.1 560-5907/8 Configuration

The following are the factory default settings for the PCI card. This configuration is restored when the Restore Factory Defaults bit is set at register location 0x12C (bit 3).

1. Mode	Generator, on
2. DAC value	8000H
3. Year	2003
4. Rate Generator	1 kPPS, on
5. Time Zone sign	+
6. Time Zone offset	0
7. Phase Compensation	0
8. Rate Synthesizer	60 PPS, off
9. Rate Synthesizer edge	Rising on time
10. Event Time Capture	External Event
11. Event Trigger edge	Rising
12. Code Out BNC	IRIG-B AM
13. Time Compare value	DAY = 1, hr = 0, min = 0, sec = 0, ms = 0, µs = 0
14. Time Compare mask	B0 (provides 100 PPS rate)

1.11.2 560-5907/8 Factory Installed Hardware Jumper Configuration

JP1: OFF - This jumper is used for IRIG-A or B with RS-422 input and provides a 120 Ω AC termination. This jumper should be OFF when using IRIG DC input mode.

JP3: Termination for Amplitude Modulated reference code input.
JP3-2 to JP3-3 (10 k Ω to GND)

JP3-1 to JP3-2 (600 Ω to GND) - Factory Default

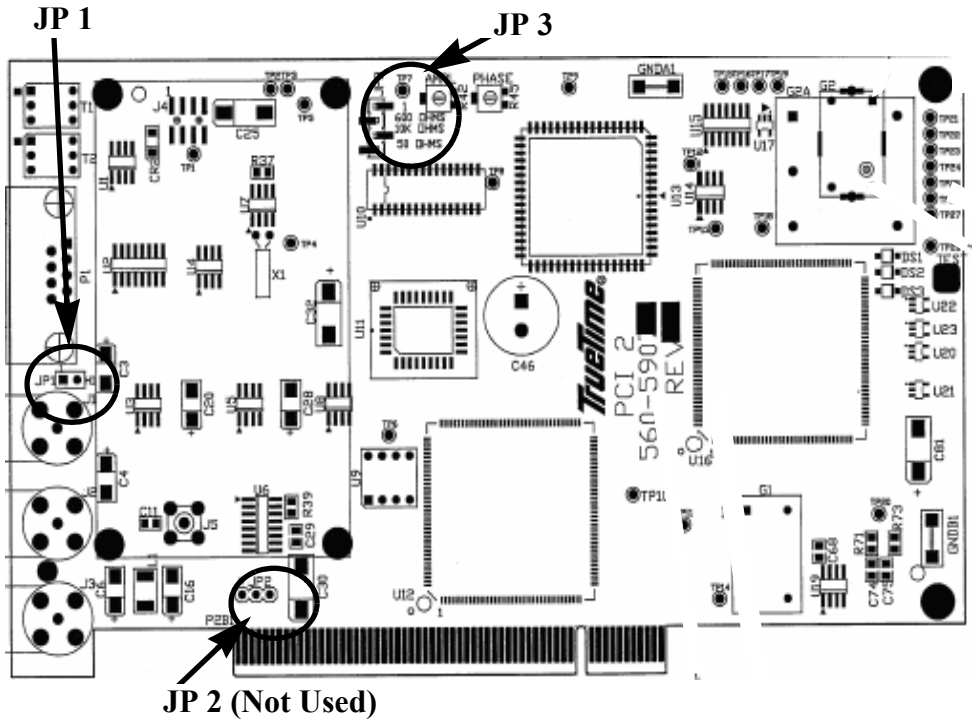
JP3-3 to JP3-4 (50 Ω to GND)

9-Pin Male D Connector (P1) Pin Assignment

PIN	Description
1	External Event / 1 PPS Input
2	GND
3	DC Reference Code Input + or TTL
4	DC Reference Code Input -
5	1 PPS Output
6	Selectable: Time Compare or Rate Synthesizer
7	Rate Generator Output
8	DC Generator Code Output + or TTL
9	DC Generator Code Output -

1.11.3 Jumper Location

Use the following drawing to locate the jumpers referred to in 1.11.2.



2

Installation

2.1 Installing the Card

This section contains installation instructions for the Model 560-5907 and 560-5908 cards, and information regarding operating modes and the use of registers to configure the card. The Model 560-5908 has the additional feature of GPS mode, which has the ability to automatically synchronize the card to UTC time.

2.1.1 Installation

Unpack the card and carefully inspect it for shipping damage. Any damage must be reported to the carrier immediately.

Record the card's serial number.

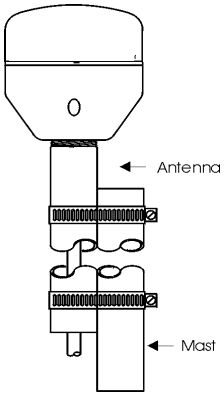
With the power OFF, install and secure the card in an empty PCI card slot. Fabricate any required I/O cables and connect them to the appropriate connectors.

2.1.2 Antenna Location and Installation (GPS only)

When selecting a site for the antenna, find an outdoor location that provides full 360-degree visibility of the horizon. In most cases, this means locating the antenna as high as possible. Any obstruction will degrade unit performance by blocking the satellite signal or causing a reflection that cancels some of the signal. Blocked signals can *significantly* increase the time for satellite acquisition, or prevent acquisition all together.

Mast Mounting

Mast top mounting is the preferred mounting method and special brackets are provided to mount the antenna to a pipe or the peak of a building. The antenna mounting mast should be 2-inch (5.08-cm) water pipe or conduit. The mast must be rigid and able to withstand high winds without flexing. Guy wires may be used to stabilize a mast longer than 10 ft. (3.048 m)



Multipath cancellation is caused by reflected signals that arrive at the antenna out of phase with the direct signal. Reflective interference is most pronounced at low elevation angles from 10 to 20 degrees above the horizon. You may extend mast height to prevent multipath cancellation. The antenna should be at least 3.28 ft. (1.0 m) from a reflecting surface.

Use of a Splitter

To run multiple units with a single 12 VDC antenna, use a splitter. Do *not* use a BNC "T" connector.

Lead-In Cable

The L1 GPS antenna is designed to operate with up to 200 ft. (60.96 m) of RG-59 coax cable. The optional Down Converter is designed to operate with up to 1,500 ft. (457.2 m) of RG-58 coaxial cable.

2.2 TTPCI Panel Software Requirements and Installation

The Symmetricom PCI cards come with the Symmetricom PCI Panel (TTPciPanel.exe) application software for Windows 95/98 and NT/2000. This software provides a graphical user interface for basic PCI card operations and can synchronize the Windows clock to the time of the card at periodic intervals (days, hours, minutes) chosen by the user.

2.2.1 Minimum System Requirements

Pentium(or faster) PC

Windows 95, 98, NT or 2000

2MB disk space

2.2.2 Installing the Software

If you currently have Symmetricom's TimeServer32 program installed on your system, you must uninstall it before installing TTPCIPanel.

To install the software, follow these steps:

1. Install the PCI board in your computer as stated in the Installation section (2.1.1) of this user manual.
2. Turn on your computer. Windows will discover your newly installed hardware. It will ask for the location of the file to initialize the new hardware.
3. Insert the Symmetricom PCIPanel CD into your computer. Change the settings on the Windows pop-up pointing to the drive the CD is located in. Windows will automatically use the Symmetricom.INF file to configure the PCI board. When Windows has finished, you are now ready to install the PCI Panel software.
4. From the **Start** menu select the **Run…** command. Using the Browse function locate the files on the CD.

Depending on your operating system double click on:

TTPciPanel_for_NT_2000.exe for the Windows NT/2000 operating environment

OR

TTPciPanel_for_95_98.exe for the Windows 95/98 operating environment

5. Select OK to run the installation programs. During installation answer the simple questions or take the defaults (suggested). The.exe files are self-extracting and will automatically load the program onto your hard drive.

2.2.3 Software Files

The following files are contained on the CD:

1. TTPciPanel_for_NT_2000.exe (use with Windows NT, 2000)
2. TTPciPanel_for_95_98.exe (use with Windows 95/98)
3. Symmetricom.inf (used when Windows discovers your newly installed card)
4. Readme.TXT (online installation instructions)

2.2.4 User Notes

TTPciPanel is an easy to use and understand program. If you have read the PCI board manual, most fields and their function are self explanatory. When in a control field and data is changed, pressing the ***ENTER*** or ***TAB*** buttons to the next control field will write the changes made into board memory. If you press ***ESC***, the change made is lost and the original value returns.

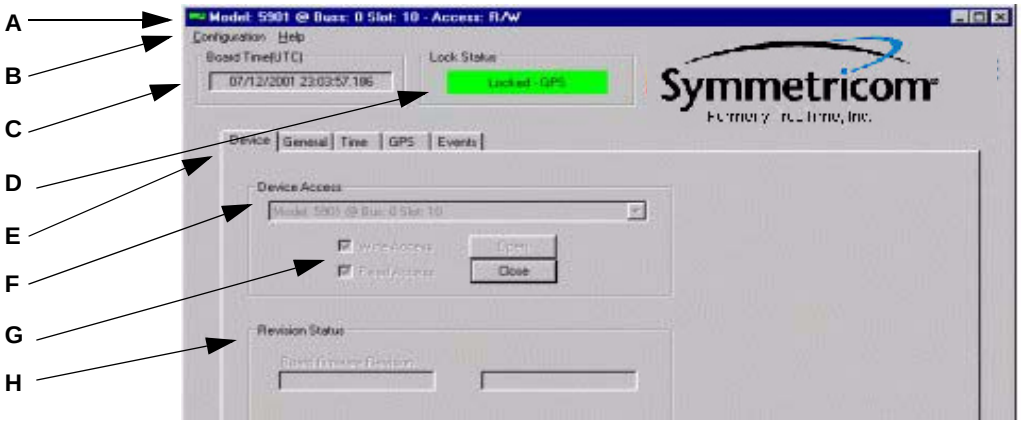
Certain functions on the menus are only available with certain model PCI cards. Some functions, fields or menus may be grayed out or otherwise not usable. For instance, the ***Save in Flash*** function in the drop-down menu is only available with PCI boards model 560-5907 and 560-5908.

Use ***Save DAC to Flash*** to quicken the card's lock time. When the card has been locked and the DAC saved, the setting will then be used as the default offset at power up.

2.2.5 Optional Software Development Kit

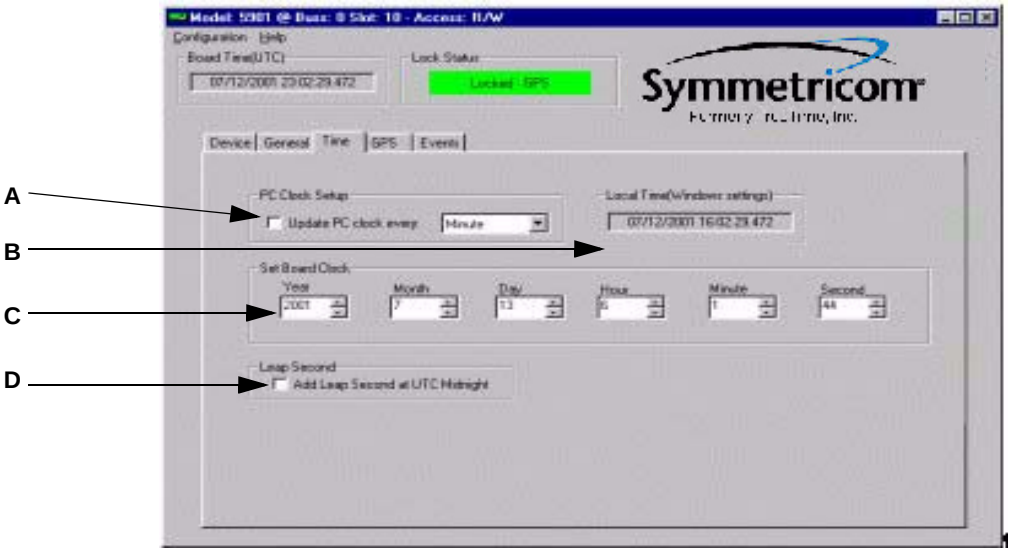
To develop applications for Symmetricom PCI cards you can order the optional Software Development Kit, SDK for PCI. This SDK also supports all Symmetricom PCI boards. Symmetricom offers this to our customers who do not wish to write their own software driver. The SDK provides the user with all the functions necessary to control and read the time from the board. This allows the user to create his own customized code for use with Symmetricom boards with a minimum of time and effort. Contact Symmetricom or visit http://www.Symmetricom.com for further detail.

Sample screen from TTPCI software-Device



A. Current board installed **B.** Drop-down menu **C.** Board Time (UTC) **D.** Lock Status
E. Menu buttons **F.** Device Access field **G.** Access boxes **F.** Revision Status

Sample screen from TTPCI software-Time



A. PC Clock Settings/Update PC clock **B.** Local Time **C.** Set Board Clock
D. Leap Second/Add Leap Second at UTC Midnight

3

Operation

3.1 General Operation

The following paragraphs describe the operation of the PCI card. They describe the operating modes, the various registers used, and how to control and configure the card. All register addresses are specified as an offset from the PCI Memory Base Address. Most features on the card may be used simultaneously. Any constraints on a specific feature in terms of its compatibility will be discussed.

The PCI card operates in either Generator Mode or Synchronized Generator Mode supplying precise time (100's of nanoseconds through thousands of years) to the host computer. The card cannot be set prior to 2000, or beyond the year 2039.

In the Generator mode the time may be started stopped and preset via the PCI bus. In this mode, the Generator time accuracy is a function of the drift rate of the on-board oscillator.

When operating as a Synchronized Generator, the output signals are synchronized to timing reference. The PCI card phase locks to the timing reference and controls the on-board oscillator to remove frequency errors. If the timing reference is lost, the PCI card continues to increment time and output timing signals based upon the previously steered on-board oscillator's frequency (flywheeling).

3.1.1 Time Preset

Year information is not encoded in the time code reference but is available over the PCI bus. To set the year, use the Time Preset function. Year data is necessary to handle end-of-year rollover correctly for leap years. Year information is saved in EEPROM and automatically increments at the end of each year.

3.1.2 Generator Mode

At turn-on, the time is based on the PCI card's real-time-clock (RTC). The RTC has the ability to run (card not powered) for over two days. The RTC accuracy is approximately one second per day.

In Generator mode, the time may be preset and the accumulation of time may be started or stopped via the Configuration Register #1. When in this mode, the PCI card runs at the rate of the on-board oscillator (timing will drift with the oscillator error).

Use the Generator mode whenever a timing source is not available or when it is necessary to start and stop the time and timing outputs (with the exception of the Rate Synthesizer). When using this mode, it is preferable to have previously used the Synchronized Generator mode connected to a timing source with known frequency accuracy, allowed the PCI card to lock to the source, and saved the DAC setting. If a synchronized DAC setting has not been previously saved, the default DAC setting is used.

3.1.3 Synchronized Generator Mode

The Synchronized Generator mode operates as a Generator that is synchronized to an external time reference. The Synchronized Generator phase locks to the time reference and disciplines the oscillator to remove frequency errors. If the reference code is lost, the Synchronized Generator continues to increment time based upon the disciplined on-board oscillator.

The Model 560-5907 (PCI-SG 2) card may be synchronized by one of the following input references:

IRIG-B AM	Year entry required
IRIG-A AM	Year entry required
IRIG-B DC	Year entry required
IRIG-A DC	Year entry required
1 PPS	Complete time entry required

The Model 560-5908 (GPS-PCI 2) card may be synchronized by any of previously listed references or by:

GPS	Automatic UTC time

3.2 PCI Card Control/Status Registers (Overview)

1. The Software Time Capture Registers are updated by writing to the low-order Freeze Register. The Time registers contain thousands of years through 100's ns. The Position Registers, used only in the GPS Synchronized mode, contain the GPS position (longitude, latitude, and elevation).
2. The Configuration Registers control the configuration of the PCI card. They are used to select the mode of operation, to select the Synchronized Generator reference, to start and stop the Generator, to preset the Generator time, to preset GPS position, to set Daylight Saving Time (DST) function, to set Event active edge, to select IRIG input codes, to set the Rate Generator output and to set the Rate Synthesizer output.
3. The Time Zone Offset Register is used to convert UTC time to local time. Local time is used for software time capture and IRIG-B output. This feature is not available with TTPCI Panel.

4. The Phase Compensation/Factory Calibration Registers are used to adjust the phase difference between the Synchronized Generator amplitude-modulated reference input and the time outputs to compensate for system delays.
5. The Diagnostic Register contains the results of the internal diagnostic tests performed at power-up and during normal operation.
6. The Event Time Registers are used to capture the time of an event. The event may be selected to be External Event or one of the following PCI card generated signals; Rate Generator, Rate Synthesizer or Time Compare.
7. The Time Compare Registers are used to program the Time Compare output.
8. The Hardware Control and Hardware Status Registers handle PCI card interrupt sources and status flags for event, time compare, rate generator, rate synthesizer, and antenna open/short.
9. The Position Preset Registers are used to preset a new position when in GPS Synchronized mode (Model 560-5908 only).
10. The Signal Level Registers contain the satellite numbers and signal levels of up to six satellites when in the GPS Synchronized mode (Model 560-5908 only).
11. The Preset Time Registers are used to set time to the level allowed for the selected modes: ms for Generator, seconds for 1 PPS Sync, Years for IRIG Sync, Epoch for GPS Sync.
12. The Rate Synthesizer Register is used to set frequency output rates.

3.3 PCI Card Registers

Data registers on the PCI card are mapped into PCI Memory Space and are used to control, configure and report information on the PCI card. All locations are described by the offset from the PCI Base Address Register 2 (the 3rd Register).

3.3.1 PCI Configuration Header Region

The PCI has a block of 64 configuration double words reserved for the implementation of its configuration registers. The first 16 double words are predefined by the PCI specification. This area is referred to as the Configuration Header Region.

To determine what devices are present, system software scans the PCI bus for the Vendor ID in each possible PCI slot. To uniquely identify the PCI card, the following registers are:

Device ID:	0x9050
Vendor ID:	0x10B5
Subsystem Vendor ID:	0x12DA
Subsystem ID:	0x5907 or 0x5908 (GPS)

3.3.2 PLX 9050 Local Configuration Registers

The PCI card's interface chip (PLX9050) has a block of 32 double word registers reserved for local configuration purposes. This area is referred to as the Local Configuration Registers and is physically mapped both to memory and to I/O addresses at run time. The memory mapped versions' base address is located at 0x10 in the Configuration Header Region (see above) and the base address for the I/O mapped version is at 0x14. Either I/O or memory read or write cycles may be used to access the LCRs. Normally, you will only access one register, the INTCSR Register, at location 0x4C.

Writing to other registers in this region runs the risk of locking up your computer or causing other unusual symptoms, requiring a power-cycle to recover.

Writing a value of xxxxxx48h to this register (0x4C) will enable the PLX9050 chip to pass along interrupts from the card if they are enabled elsewhere. The card is normally shipped with this value pre configured, however, it is possible that this value has been changed from the default and you will need to know how to set it back. Note that the value xxxxxx08h will disable all interrupts.

3.3.3 Hardware Control Register

This register (see next page) is used to control the interrupts and clear the signal status bits that are generated by the PCI card. Note that the status bits are generated regardless of the state of the interrupt mask bits in this register.

Select PCI interrupt sources via the Hardware Control Register located at offset 0xF8. Any combination of sources in the following table may be selected. The Event, Time Compare, Rate Generator and Rate Synthesizer flags are always available in the Hardware Status Register and can be un-masked, via bits 3, 4, 5 and 7 to generate interrupts. The Status bits are cleared via bits 0, 1, 2 and 6 (writing a 1 to these bits generates a 1-cycle clear pulse). In addition to this register, you may also need to program the INTCSR register at offset 0x4C in the PLX9050 chip (see prior section PLX 9050 Local Configuration Registers).

Hardware Control Register

PCI Offset	Bits 7-4	Bits 3-0
0XF8[P]	Interrupt and Status Flag Control [1]	
0xF9	Undefined	Undefined
0xFA	Undefined	Undefined
0xFB	Undefined	Undefined

Notes:
P: PCI Quad Address (base address of four ascending contiguous bytes)
1: Interrupt and Status Flag Control
Bit 7: Rate Synthesizer Interrupt Mask (0=Interrupt Disabled, 1= Enabled
Bit 6: Rate Synthesizer Status Clear
Bit 5: Rate Generator Interrupt Mask (0= Interrupt Disabled, 1= Enabled)
Bit 4: Time Compare Interrupt Mask (0=Interrupt Disabled, 1= Enabled)
Bit 3: Event Interrupt Mask (0= Interrupt Disabled, 1= Enabled)
Bit 2: Rate Generator Status Clear
Bit 1: Time Compare Status Clear
Bit 0: Event Status Clear

All status clear bits operate the same. When a 1 is written to the status clear bit, the corresponding bit at location 0xFE (Status Flag) is cleared.

3.3.4 Software Time Capture Register

This register (see next page) is used to obtain a software time capture from the card. In order to obtain time, write any value to location 0xFC. This causes the current time, compensated by the local offset and daylight saving time, to be written to this register. The time is stable and ready to read when the Software Time Ready bit is set in the Status Flags location (0xFE). Writing location 0xFC causes the Software Time Ready bit to be cleared. The time delay from the write of 0xFC to the Ready bit being set is a maximum of 150 ns. Time can be read immediately following the write to 0xFC (not waiting for the status flag). The Time Registers start at offset 0xFC and contain packed BCD data, except for the Status bits.

Software Time Capture Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0xFC[P1]	Tens microseconds	Unit microseconds
0xFD	Unit milliseconds	Hundreds microseconds
0xFE	Antenna Status[2]	Status Flags[2]
0xFF	100's of nanoseconds	Undefined
0x100[P]	Hundreds milliseconds	Tens milliseconds
0x101	Tens seconds	Unit seconds
0x102	Tens minutes	Unit minutes
0x103	Tens hours	Unit hours
0x104[P]	Tens days	Unit days
0x105	Lock Status[3]	Hundreds days
0x106	Tens years	Unit years
0x107	Thousands years	Hundreds years

Notes: Time Nibbles are BCD, status nibbles are bits
P: PCI Quad Address (base address of four ascending contiguous bytes)
1: Writing any value to location 0xFC updates time and position
2: Antenna/Status Flags
The explanation for these two nibbles is contained in the following Hardware Status Register section
3: Lock Status
Bit 7: Undefined
Bit 6: Phase Locked to Input REF (0 = Not Locked, 1 = Locked). Locked = timing specification is met.
Bit 5: Input Valid (0 = Not Valid, 1 = Valid). Valid = Time is obtained from reference and is correct.
Bit 4: GPS Lock (0 = Not Locked, 1 = Locked). Locked = All necessary GPS info has been obtained.

3.3.5 Hardware Status Register

The register at memory location 0xFE contains status related to the software time, antenna, and generated signals. The antenna bits are set automatically based on the state of the antenna connection. If the card is not a GPS model (560-5908), both bits will be '0'.

The status flags are set automatically whenever the corresponding signal occurs (Event, Time Compare, Rate Generator and Rate Synthesizer). These flags are always available as status and can be un-masked, via the Hardware Control Register at location 0xF8, to generate interrupts.

Note that if the event source is selected to be anything other than External Event, the event flag will go active simultaneously with the flag corresponding to the event source. If External Event is selected as the source, then the event flag will go active only with the occurrence of the External Event.

The signal status flags are set regardless of the interrupt mask bit. The status flags are cleared by a write to the corresponding clear bit in the Interrupt and Status Flag Control byte at location 0xF8.

The Software Time Ready flag is set by software when the Software Time Register is ready to be read because time is latched into these registers by the 100 ns system clock. This bit is always set.

Hardware Status Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0xFE	Antenna Status[1]	Status Flags[2]

Notes:
1: Antenna Status
Bit 7: Undefined
Bit 6: Software Time Ready (1 = Ready, Cleared when location 0xFC is written)
Bit 5: GPS Antenna Shorted (0 = Shorted, 1 = Not Shorted)
Bit 4: GPS Antenna Open (0 = Open, 1 = Not Open)
2: Status Flags
Bit 3: Rate Synthesizer (1 = rising edge occurred)
Bit 2: Rate Generator (1 = rising edge occurred)
Bit 1: Time Compare (1 = rising edge occurred)
Bit 0: Event (1 = selected edge occurred)
(Edge and source are selected by the Event Time Capture Control byte, location 0x12E)
(Individual status bits are cleared by writing the corresponding clear bit in location 0xF8)

3.3.6 Antenna Position Register (560-5908 only)

This register is used to obtain GPS antenna position from the 560-5908 PCI card. The antenna position is provided at locations 0x108 - 0x11F. All Antenna Position values are BCD except for the direction bytes, which are ASCII values indicating the direction.

It is recommended that this register be read twice and compared to verify a correct position has been read. This double read is strongly recommended in mobile applications.

Antenna Position Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x108[P]	Latitude Tens Degrees	Latitude Unit Degrees
0x109	0	Latitude Hundreds Degrees
0x10A	Latitude Tens Minutes	Latitude Unit Minutes
0x10B	Latitude North / South byte (ASCII 'N' 0x4E or 'S' 0x53)	
0x10C[P]	0	Latitude Tenths Seconds
0x10D	Latitude Tens Seconds	Latitude Unit Seconds
0x10E	Longitude Tens Degrees	Longitude Unit Degrees
0x10F	0	Longitude Hundreds Degrees
0x110[P]	Longitude Tens Minutes	Longitude Unit Minutes
0x111	Longitude East / West byte (ASCII 'E' 0x45 or 'W' 0x57)	
0x112	0	Longitude Tenths Seconds
0x113	Longitude Tens Seconds	Longitude Unit Seconds
0x114[P]	Altitude Tens Kilometers	Altitude Unit Kilometers
0x115	Altitude Sign byte (ASCII '-' 0x2D or '+' 0x2B)	
0x116	Altitude Unit Meters	Altitude Tenths Meters
0x117	Altitude Hundreds Meters	Altitude Tens Meters

Notes: Position is BCD nibbles except Latitude N/S, Longitude E/W and Altitude +/- which are ASCII
Writing any value to location 0xFC updates the position
P: PCI Quad Address (base address of four ascending contiguous bytes)

3.3.7 Configuration #1 Register

This register is used to control the operating mode and the Rate Generator. It also controls time and position presets as well as Daylight Saving Time enable, which is available in all modes. If you have requested a preset time, read location 0x118. When the 0x04 bit is cleared, the time has been set in the Preset Time Register. After a mode change, allow 60 seconds for the PCI card to reinitialize before checking lock status.

The Rate Generator outputs a signal on pin 7 of the 9-pin connector, and output may be selected on J1 "CODE OUT" BNC, with one of nine fixed rates. The Rate Generator signal is synchronous with the board timing and the rising edge is on-time. Write a BCD value to the upper nibble of the Configuration Register to select the rate of the output signal. The Rate Generator bit of the Hardware Status Register (0xFE) indicates when a Rate Generator pulse has occurred.

Configuration #1 Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x118[P]	Time Source Control [1]	
0x119	Timecode Control [2]	
0x11A	Undefined	Undefined
0x11B	Rate Generator [3]	Undefined

Notes: P = PCI Quad Address (base address of four ascending contiguous bytes)

1: Time Source Control

Bit 7: GPS Preset Position Ready (1 = Use position in Preset / Position register)
Bit 6: 1 PPS reference (0= Disabled, 1 = Enabled)
Bit 5: GPS reference (0= Disabled, 1 = Enabled)
Bit 4: Timecode reference (0= Disabled, 1 = Enabled)
Bit 3: Generator Control (0 = Run, 1 = Stop, valid only when bit 0 is 0)
Bit 2: Time Preset Ready (1 = Use time in Time Preset register)
Bit 1: Daylight Saving Time (0 = Disabled, 1 = Enabled)
Bit 0: Time Mode Select (0 = Generator, 1 = Synchronized Generator)

2: Timecode Control

Bit 7: Timecode Input to Read (0 = AM, 1 = DC)
Bits 6-3: Unused
Bits 2-0: Input Timecode Format
0x0: IRIG-B 0x1: IRIG-A

3: Rate Generator Control (all rates PPS)

0x0: Disabled 0x1: 10K 0x2: 1K
0x3: 100 0x4: 10 0x5: 1
0x6: 100K 0x7: 1M 0x8: 5M
0x9: 10M

3.3.8 Diagnostic Register

The Diagnostic Register at 0x11C contains the results of a diagnostic test that is done at power-up and during normal operation. The bits in the least significant byte represent a potential error. If the bit is set, that error has occurred.

When the PCI card is used in Synchronized Generator mode with an IRIG input and the input code is from Symmetricom equipment that has Time Quality Flags in the code; the register at location 0x11D will indicate the input source Time Quality status. If the "Use Time Quality" bit is set at location 0x12C, the PCI card will set the "Input Signal Valid" bit in the "Lock Status" locations to "Not Valid" if the incoming code is unlocked. Note that the PCI card will still phase lock to the input code. The IRIG-B output from the PCI card will include the input reference's Time Quality bits from the same source when location 0x12C bit 1 is set; when not set, the Time Quality bits are stripped.

The oscillator status, available in the Diagnostic Register at offset 0x11E, contains a 16-bit value representing the current output of the digital-to-analog converter (DAC). The DAC output controls the frequency of the crystal oscillator used as the time base for the PCI card. This output ranges from 0x0000 to 0xFFFF hexadecimal. This value may vary from its midrange value (0x8000) significantly, depending on the accuracy, stability of the reference frequency, the ambient temperature, and oscillator aging.

Diagnostic Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x11C[P]	Undefined	Background Test Status[1]
0x11D	Source Time Quality Flags[2]	
0x11E	DAC Setting (Low byte)[3]	
0x11F	DAC Setting (High byte)[3]	

Notes: P= PCI Quad Address (base address of four ascending contiguous bytes)

1: Background Test Status
Bit 3: 1 indicates Hardware Failure
Bit 2: 1 indicates DAC setting near limit
Bit 1: 1 indicates on-board RAM Failure
Bit 0: 1 indicates Processor Clock Failure

2: Source Time Quality Flags (Not locked and TQ Fault asserted = 1)
Bit 7: Symmetricom IRIG Source Time Quality Level 4
Bit 6: Symmetricom IRIG Source Time Quality Level 3
Bit 5: Symmetricom IRIG Source Time Quality Level 2
Bit 4: Symmetricom IRIG Source Time Quality Level 1
Bit 3: Symmetricom IRIG Source Not Locked
Bit 2-0: Undefined.

3: DAC Setting
This is the 16-bit setting used to steer the 10 MHz oscillator

3.3.9 Time Zone Offset Register

This register provides time zone offset (Local Time Correction) from UTC. The PCI card's Software Time Capture, Event Capture and IRIG-B output use local time. This feature is available in all modes but cannot be accessed from the TTPCI Panel. This value is always set to 0 when the Symmetricom driver is loaded.

Time Zone Offset Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x120^{P}	Tens Minutes	Unit Minutes
0x121	Tens Hours	Unit Hours
0x122	Sign byte (ASCII '-' 0x2D or '+' 0x2B)	
0x123	Undefined	Undefined
Notes: P = PCI Quad Address (base address of four ascending contiguous bytes) Allowable offset is +/- 12:59 Setting in this register is used only in Synchronized Generator modes		

3.3.10 Phase Compensation / Factory Calibration Registers

The Phase Compensation register provides the ability to correct the PCI card's timing outputs for phase delay caused by cabling. The value in this register will be used to offset fixed phase errors, either positive or negative. The value written to 0x125 and 0x124 must be a sixteen-bit signed binary number representing microseconds of compensation. The range of compensation is from -800 to +800 µs. Generally, phase compensation is a positive number. Negative numbers should be used only for test purposes. Phase Compensation may also be adjusted at the 100 ns level using the register at location 0x126.

Factory calibration is performed to compensate for IRIG-AM circuit delays. The procedure for calibration requires an IRIG-A or B amplitude modulated reference and a 1 PPS signal from the same source (so that the signals are on time with one another). The 1 PPS input is connected to the External Event input on the PCI card. Note that the PCI card has separate calibration values for IRIG-A and IRIG-B (stored in EEPROM).

Phase Compensation/Factory Calibration Registers

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x124[P]	Phase Compensation (low byte)[1]	
0x125	Phase Compensation (high byte)[1]	
0x126	Phase Compensation 100 ns[2]	
0x127	Factory Calibration[3]	

Notes: P= PCI Quad Address (base address of four ascending contiguous bytes)

1: Phase Compensation (microseconds)
This value is a signed integer. Resolution is 1µs, range is +/- 800 µs.

2: Phase Compensation (100's ns)
This byte can hold a value of 0-9 to add in as 100s of ns phase compensation. It is just a Magnitude value and has the same sign as the µs.

3: Factory Calibration
A value of 'A' (hex 41) causes the card to determine the delay from an IRIG-A AM source to a 1 PPS signal and save that value in EEPROM.
A value of 'B' (hex 42) causes the card to determine the delay from an IRIG-B AM source to a 1PPS signal and save that value in EEPROM.
When either an 'A' or a 'B' is entered, the system responds by checking all input parameters for validity before setting the calibration. If an error is detected, an error message is reported:

1. Source Error, a non-IRIG source was selected as the reference
2. The selected source does not match the calibration character
3. The event source was not selected to be external event
4. The IRIG input was not valid.
5. The phase compensation is not set to 0.
6. The time differential between the 1 PPS and the IRIG on-time mark was too large (45 µs for IRIG-B, 145 µs for IRIG-A).
7. The 1 PPS on-time mark occurs after the IRIG on-time mark.

If no errors are detected, the software sets the value at this location to 0x40 to indicate that a calibration is being performed. Once the calibration has been completed, the value is set to 0.

3.3.11 Rate Synthesizer Register

The user can configure a Rate Synthesizer that will output a frequency from 1 to 1,000,000 PPS in 1 PPS increments. The Rate Synthesizer does not have a default output connector, but can be directed to either pin 6 of the 0-9 or to the Code Out BNC , or both, take using the Configuration #2 Register.

The Rate bit of the Hardware Status Register (0xFE) indicates when a Rate Synthesizer pulse has occurred. The Rate Synthesizer signal may be configured to produce an interrupt to the PCI host processor on the rising edge at the output frequency (see location 0xF8).

This register is used to set only the frequency. Run\Stop, on-time edge and output control are done in Configuration #2 Register.

Rate Synthesizer Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x128[P]	Rate Synthesizer Frequency (low byte) [1]	
0x129	Rate Synthesizer Frequency (low middle byte) [1]	
0x12A	Rate Synthesizer Frequency (high middle byte) [1]	
0x12B	Rate Synthesizer Frequency (high byte) [1]	
Notes: P= PCI Quad Address (base address of four ascending contiguous bytes) **1: This value is an unsigned long integer.** Resolution is 1 PPS, range is 1 to 1 MPPS		

3.3.12 Configuration #2 Register

Leap Second and other card control items are set with the registers at locations 0x12C through 0x12F.

Leap Second correction is available only in Synchronized Generator modes. When set, the unit will add an extra second at the end of the current day. The bit will clear automatically after the leap second has occurred. Note that the second added is second 60. When using Symmetricom's SDK and the TTPCI Panel program, the Software Time Capture or Event Time Capture will display two consecutive second 59's when a leap second occurs. This is due to the limitations of some computer systems accepting second 60. The PCI card's IRIG output provides a 60^{th} second.

Configuration #2 Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x12C[P]	Miscellaneous Control [1]	
0x12D	Rate Synthesizer Control [2]	
0x12E	Event Time Capture Control [3]	
0x12F	Code Out (J1) BNC Source Select [4]	

Notes: P = PCI Quad Address (base address of four ascending contiguous bytes)

1: Miscellaneous Control

Bit 5: Restore factory defaults (from FLASH, self clears when finished)
Bit 4: Restore EEPROM values (self clears when finished)
Bit 3: Save Current setup (stores to EEPROM, self clears when finished)
Bit 2: Setting this bit saves the current DAC Setting (EEPROM, self clears when finished)
Bit 1: Use Time Quality bits from Input (affects Input Valid bit in Lock Status locations)
Bit 0: Setting this bit causes a leap second (second = 60) to follow 23:59:59 Local Time

2: Rate Synthesizer Control

Bit 3: Synthesizer signal available on D9 pin-6 instead of Time Compare (1 = Synthesizer)
Bit 2: Synthesizer on-time Edge (0 = Falling, 1 = Rising)
Bit 1: Synthesizer Load (Setting this bit loads the Rate Synthesizer register value)
Bit 0: Synthesizer Output Enable (0 = Stop, 1= Run)

3: Event Time Capture Control

Bits 1-0: Event Source
0x0: External Event 0x1: Rate Synthesizer
0x2: Rate Generator 0x3: Time Compare
Bit 2: Event Trigger Edge (0 = Falling, 1 = Rising)

4: Code Out BNC (J1) Source Select

0x0: IRIG-B AM 0x1: IRIG-B DC 0x2 Rate Generator 0x5: 1 PPS
0x3: Rate Synthesizer 0x4 Time Compare

3.3.13 Time Compare Register

This register is used to set the time (or rate) that a time compare pulse is generated. When the time is equal to the value in the Time Compare registers, an active high, one ms pulse, is generated. The pulse can be directed to either pin 6 of the D9 or to the Code Out BNC, or both, using the Configuration #2 Register. Time Compare may be used to generate a PCI interrupt (see location 0xF8). The Time Compare bit at location 0xFE indicates when a Time Compare has occurred.

Load the desired time of the time compare in the Time Compare Registers. The compare mask nibble is a hexadecimal number between 0x0 and 0xB. The compare mask limits the data used in the time compare operation. For example, if the mask is 0x0, all data (hundreds of days through microseconds) are compared. If the mask is a 0x1, then hundreds of days is ignored. Values from 0xC to 0xF disable Time Compare output.

The compare mask can be used to output pulses at regular time intervals. For example, a mask value of 0xB causes a comparison of the microseconds through milliseconds data resulting in a pulse every ten milliseconds.

Time Compare Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x138[P]	Tens microseconds	Unit microseconds
0x139	Unit milliseconds	Hundreds microseconds
0x13A	Hundreds milliseconds	Tens milliseconds
0x13B	Tens seconds	Unit seconds
0x13C[P]	Tens minutes	Unit minutes
0x13D	Tens hours	Unit hours
0x13E	Tens days	Unit days
0x13F	Compare Mask[1]	Hundreds days

Notes = Time Nibbles are BCD, mask nibble is bit field
P = PCI Quad Address (base address of four ascending contiguous bytes)

1: Compare Mask

0x0: Compare Hundreds Day through Unit microseconds (pulse every 1 year)
0x1: Compare Tens Day through Unit microseconds (pulse every 100 days)
0x2: Compare Unit Day through Unit microseconds (pulse every 10 days)
0x3: Compare Tens Hour through Unit microseconds (pulse every 1 day)
0x4: Compare Unit Hour through Unit microseconds (pulse every 10 hours)
0x5: Compare Tens Minute through Unit microseconds (pulse every 1 hour)
0x6: Compare Unit Minute through Unit microseconds (pulse every 10 minutes)
0x7: Compare Tens Second through Unit microseconds (pulse every 1 minute)
0x8: Compare Unit Second through Unit microseconds (pulse every 10 seconds)
0x9: Compare Hundreds millisecond through Unit microseconds (pulse every 1 second)
0xA: Compare Tens millisecond through Unit microseconds (pulse every 100 ms)
0xB: Compare Unit millisecond through Unit microseconds (pulse every 10 ms)

3.3.14 Preset Time Register

This register is used to set PCI card time in all modes. The locations shown in the table below are used to preset the time as allowed by operating modes. First, write packed BCD milliseconds through thousands of years into the Preset Time Registers, afterwards, set the Preset Time Ready bit of the Configuration Register, which will automatically clear once the preset time is loaded.

Preset Time Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x158[P]	Undefined	Undefined
0x159	Unit milliseconds	Undefined
0x15A	Hundreds milliseconds	Tens milliseconds
0x15B	Tens seconds	Unit seconds
0x15C[P]	Tens minutes	Unit minutes
0x15D	Tens hours	Unit hours
0x15E	Tens days	Unit days
0x15F	Undefined	Hundreds days
0x160[P]	Tens years	Unit years
0x161	Thousands years	Hundreds years
0x162	Undefined	Undefined
0x163	Undefined	Undefined
Notes: Nibbles are BCD P = PCI Quad Address (base address of four ascending contiguous bytes)		

The time that is loaded depends on the mode:

GPS Sync Gen: Years are used to establish Epoch. To set the Epoch to the years 2000-2019, the year 2000 must be entered.

IRIG Sync Gen: Years only

PPS Sync Gen :Time from Years to Seconds

Generator : Time from Years to Milliseconds

The time from Years to Seconds is absolute and changes as indicated. The Milliseconds Preset Time is relative and adjusts the output on-time mark by the requested time. For example, if the milliseconds time is set to 103, the on-time mark will occur 103 ms later.

3.3.15 Preset Position Register (560-5908 only)

This register is used to set the GPS Antenna position prior to a fix being obtained. The GPS receiver will auto locate within 20 minutes whether or not this register is used (see Section 1.8). An entry in this register will only speed up the time fix by at most ten minutes. This register should be used carefully, because an invalid position entry may cause the receiver to not obtain any lock until power is cycled.

If this register is used, the GPS Preset Position Ready bit in the Configuration #1 register must be set after the position is entered.

Preset Position Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x164[P]	Latitude Tens Degrees	Latitude Unit Degrees
0x165	0	Latitude Hundreds Degrees
0x166	Latitude Tens Minutes	Latitude Unit Minutes
0x167	Latitude North / South byte (ASCII ‘N’ 0x4E or ‘S’ 0x53)	
0x168[P]	0	Latitude Tenths Seconds
0x169	Latitude Tens Seconds	Latitude Unit Seconds
0x16A	Longitude Tens Degrees	Longitude Unit Degrees
0x16B	0	Longitude Hundreds Degrees
0x16C[P]	Longitude Tens Minutes	Longitude Unit Minutes
0x16D	Longitude East / West byte (ASCII ‘E’ 0x45 or ‘W’ 0x57)	
0x16E	0	Longitude Tenths Seconds
0x16F	Longitude Tens Seconds	Longitude Unit Seconds
0x170[P]	Altitude Tens Kilometers	Altitude Unit Kilometers
0x171	Altitude Sign byte (ASCII ‘-’ 0x2D or ‘+’ 0x2B)	
0x172	Altitude Unit Meters	Altitude Tenths Meters
0x173	Altitude Hundreds Meters	Altitude Tens Meters
Notes: Position Nibbles are BCD, Sign bytes are ASCII P= PCI Quad Address (base address of four ascending contiguous bytes)		

3.3.16 Event Time Capture Register

This register is used to capture the time when an event occurs. The Event may be selected to be External, Time Compare, Rate Generator or Rate Synthesizer. The on-time edge of the event may also be selected (0x12E bit 2). When a capture is made, time from 100's of nanoseconds through years is saved and available to the host in packed BCD format. A flag in the Hardware Status Register (0xFE) sets when the Event Time is available. The time delay from the Event edge and the Event ready bit being set is a maximum of 150 ns.

Only the oldest event time is stored and will not change regardless of another event occurring. To latch time for a new event. The Event Status flag at location 0xFE must be cleared by writing the Event Clear bit at location 0xF8.

The Event can generate a PCI interrupt (see 0xF8).

Event Time Capture Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x174[P]	Tens microseconds	Unit microseconds
0x175	Unit milliseconds	Hundreds microseconds
0x176	Hundreds milliseconds	Tens milliseconds
0x177	Tens seconds	Unit seconds
0x178[P]	Tens minutes	Unit minutes
0x179	Tens hours	Unit hours
0x17A	Tens days	Unit days
0x17B	Lock Status[1]	Hundreds days
0x17C[P]	Tens years	Unit years
0x17D	Thousands years	Hundreds years
0x17E	100's of nanoseconds	Undefined
0x17F	Undefined	Undefined

Notes: Time and Position Nibbles are BCD, status nibbles are bits
P= PCI Quad Address (base address of four ascending contiguous bytes)
1: Lock Status
Bit 7: Undefined
Bit 6: Phase Locked to Input Ref (0 = Not Locked, 1 = Locked. Indicates that the timing specification is met)
Bit 5: Input Valid (0 = Not Valid, 1 = Valid. Indicates that time is obtained from reference and is correct.)
Bit 4: GPS Lock (0 = Not Locked, 1 = Locked. Indicates all necessary GPS info has been obtained.)

3.3.17 Satellite Signal Strength Register (560-5908 only)

This register indicates the signal levels of the satellites being used in the timing solution. Signal strength is provided at locations 0x198 through 0x1AF. A maximum of six satellites are monitored and the information for each satellite is contained in four locations. The first location provides the satellite SV number; the last two locations contain the satellite signal strength. The satellites are in no particular order. Satellites in this register description are assigned alphabetic designations to indicate that there is no relationship between their relative position in the register and their SV Number. Before reading satellite data, the satellite update status (location 0x1B0) should be checked. If the location is non-zero, the satellite data should not be read. Following a read of the satellite data, location 0x1B0 should be checked again. If the location is non-zero, the satellite data should be discarded and read again when location 0x1B0 is zero. When the flag byte is set, it indicates that either the information is not available, or it is being updated. The signal level information is updated approximately every 10 seconds. Signal levels are normally positive. If it is zero, then that satellite has not yet been acquired, or is not currently being tracked. The signal level is a measure of the signal strength after correlation or de-spreading. A good signal level magnitude is five or more.

Satellite Signal Strength Register

PCI Offset	Bits 7 – 4	Bits 3 – 0
0x198^{P}	Tens SV Number, Satellite A	Unit SV Number, Satellite A
0x199	Undefined	Undefined
0x19A	tenths signal level, Satellite A	hundredths signal level, Satellite A
0x19B	Tens signal level, Satellite A	Unit signal level, Satellite A
0x19C^{P}	Tens SV Number, Satellite B	Unit SV Number, Satellite B
0x19D	Undefined	Undefined
0x19E	tenths signal level, Satellite B	hundredths signal level, Satellite B
0x19F	Tens signal level, Satellite B	Unit signal level, Satellite B
0x1A0^{P}	Tens SV Number, Satellite C	Unit SV Number, Satellite C
0x1A1	Undefined	Undefined
0x1A2	tenths signal level, Satellite C	hundredths signal level, Satellite C
0x1A3	Tens signal level, Satellite C	Unit signal level, Satellite C
0x1A4^{P}	Tens SV Number, Satellite D	Unit SV Number, Satellite D
0x1A5	Undefined	Undefined
0x1AA	tenths signal level, Satellite D	hundredths signal level, Satellite D
0x1A7	Tens signal level, Satellite D	Unit signal level, Satellite D
0x1A8^{P}	Tens SV Number, Satellite E	Unit SV Number, Satellite E

Satellite Signal Strength Register

0x1A9	Undefined	Undefined
0x1AA	tenths signal level, Satellite E	hundredths signal level, Satellite E
0x1AB	Tens signal level, Satellite E	Unit signal level, Satellite E
0x1AC[P]	Tens SV Number, Satellite F	Unit SV Number, Satellite F
0x1AD	Undefined	Undefined
0x1AE	tenths signal level, Satellite F	hundredths signal level, Satellite F
0x1AF	Tens signal level, Satellite F	Unit signal level, Satellite F
Notes: Satellite Number and signal strength nibbles are BCD P: PCI Quad Address (base address of four ascending contiguous bytes)		

3.3.18 Satellite Signal Strength Update Status

This register is used to indicate when satellite signal levels are static and can be read.

Satellite Signal Strength Update Status

PCI Offset	Bits 7-4	Bits 3-0
0x1B0[P]	Update Status	Update Status
0x1B1	Undefined	Undefined
0x1B2	Undefined	Undefined
0x1B3	Undefined	Undefined
Notes: Satellite Number and signal strength nibbles are BCD P = PCI Quad Address (base address of four ascending contiguous bytes) **1: Update Status** When non-zero, satellite data is being updated and is not valid		

3.3.19 IRIG AM AGC Delays

This register reports the Factory Calibration values obtained for both IRIG-A and B AM delays. Values are the phase compensation applied to each code. This register is READ only.

IRIG AM AGC Delay

PCI Offset	Bits 7 – 0
0x1B4	IRIG-B AM microseconds delay
0x1B5	IRIG-B AM nanoseconds delay
0x1B6	IRIG-A AM microseconds delay
0x1B7	IRIG-A AM nanoseconds delay

3.3.20 Software Version Register

This register reports the PCI card software version. This register is READ only.

Software Version Register

PCI Offset	Bits 7 – 0
0x1BC	Software Version Major
0x1BD	Software Version Minor
0x1BE	Software Version Test
0x1BF	Unused

3.4 Examples

After a mode change, allow 60 seconds for the PCI card to reinitialize before checking the lock status.

3.4.1 Generator Mode

Selecting the Mode

First, select the Generator mode. To run this mode, write the value 0x00 to location 0x118. To stop the Time and Rate Generator outputs write the value 0x08 to location 0x118.

Setting Time

Write the current time from ms to year (in BCD) to the Preset Time Register locations 0x158 to 0x161. Set the preset time bit by (OR)ing the contents of location 0x118 with a 0x04.

Status

When in Generator mode, there is no status information available. If you have requested a preset time, read location 0x118. When the 0x04 bit is cleared, the time has been set to the time in the Preset Time Register. Check the Background Test bits located in the diagnostic register (0x11C) to find a background test error.

Start/Stop

The Generator accumulates time when the Generator Stop bit of the Configuration Register is clear. The Generator stops when this bit is set. This bit is valid only in Generator mode.

Registers Used in Generator Mode

Configuration Register #1: Location 0x118

Preset Time Register: Locations 0x158 to 0x161

Diagnostic Register: Location 0x11C

3.4.2 Synchronized Generator - IRIG AM

This feature interprets the time by an input AM time code signal and steers the oscillator to the timing provided by that signal. The time provided by the time code is interpreted as UTC for use by the card. The supported time codes are given below.

Procedure

1. Connect the Input AM Signal to the time code BNC located on the PCI card panel.
2. Select the specific AM time code to interpret. Write the value that corresponds to the desired time code to location 0x119.

   Use the following values:

   IRIG-B: 0

   IRIG-A: 1
3. To select the Time Code Synchronized Generator mode, write 0x11 to location 0x118.
4. To set the Year, write the current year in BCD to 0x160 (tens and unit) and 0x161 (thousands and hundreds).
5. Set the preset time bit by (OR)ing the contents of location 0x118 with a 0x04.
6. When Phase Lock is indicated, save the DAC setting (optional). Write 0x04 to location 0x12C.

The EEPROM has limited write cycles (100,000)

Status

To verify the timing status, first write any value to location 0xFC, then check the two bits in the Lock Status nibble located at 0x105 of the Software Time Request Register.

The two bits are:

Bit 5: Input Signal Valid. When set, three consecutive code frames have been detected and agree.

Bit 6: Phase Lock. When set, the output signal timing matches the input signal timing +/-3 µs.

If the preset time has been requested, read 0x118. When the 0x04 bit is cleared, the PCI card time has been set to the time in the Preset Time Register. Check location 0x110C in the diagnostic register of the Background Test to determine any errors.

Registers Used in Synchronized Generator mode (IRIG-AM)

Configuration Register #1: Locations 0x118, 0x119

Preset Time Register (Year only): Locations 0x160, 0x161

Lock Status Register: Location 0x105

Configuration Register #2: Location 0x12C (Optional DAC save)

Diagnostic Register: Location 0x11C

3.4.3 Synchronized Generator - IRIG DC

This feature interprets the time by an input DC time code signal and steers the oscillator to the timing provided by that signal. Use this mode whenever the best available timing source is a DC time code signal. The time provided by the time code is interpreted as UTC for use by the card. The supported Timecodes are given below.

To use RS-422 logic levels, input DC-shift code at pins 3(+) and 4(-) of the 9-pin connector. If it is desired to not use 120 ohm termination, remove the jumper on JP1. To use TTL logic levels, connect DC-shift time code to pin 3 of the 9-pin connector with jumper JP1 OFF. Connect amplitude-modulated time code at the rear panel BNC labeled "CODE IN". Match the impedance of the input code using JP2.

Procedure

1. Connect the input DC code to the D9 connector. If the input signal is RS-422 level, connect the positive to pin 3 and negative pin to 4. If the input signal is TTL level, connect the input signal to pin 3 and ground to pin 2.
2. Select the specific DC time code to interpret. Write the value that corresponds to the desired time code to location 0x119.

   Use the following values:

   - IRIG-B 80
   - IRIG-A 81

3. To select the Time Code Synchronized Generator mode, write 0x11 to location 0x118.
4. To set the Year, write the current year in BCD to 0x160 (tens and unit) and 0x161 (thousands and hundreds).
5. Set the preset time bit by (OR)ing the contents of location 0x118 with a 0x04.
6. When Phase Lock is indicated, save the DAC setting (optional). Write 0x04 to location 0x12C.

The EEPROM has limited write cycles (100,000)

Status

To check the timing status, first write any value to location 0xFC, then examine the two bits in the Lock Status nibble located at 0x105 of the Software Time Request Register. The two bits are:

Bit 5: Input Signal Valid. When set, three consecutive frames have been detected and agree.

Bit 6: Phase Lock. When set, the output signal timing matches the input signal timing +/-1 μs.

If the preset time has been requested, read 0x118. When the 0x04 bit is cleared, the PCI card time has been set to the time in the Preset Time Register. Check location 0x110C in the diagnostic register of the Background Test to determine any errors.

Registers Used in Synchronized Generator mode (IRIG DC)

Configuration Register #1:	Locations 0x118, 0x119
Preset Time Register (Year only):	Locations 0x160, 0x161
Lock Status Register:	Location 0x105
Configuration Register #2:	Location 0x12C (Optional DAC save)
Diagnostic Register:	Location 0x11C

3.4.4 Synchronized Generator – 1 PPS

This feature steers the oscillator to the timing provided by the rising edge of a 1 PPS input signal.

When this mode is invoked, the card does not support use of an external event for event time capture.

Procedure

1. Connect the 1PPS input signal to the D9 connector, pin 1.
2. Select 1PPS Synchronized Generator mode. Write the value 0x41 to location 0x118.
3. To set the time, write locations 0x15B through 0x161. Set the preset time bit by (OR)ing the contents of location 0x118 with a 0x04. Time should be set on the next occurrence of the 1 PPS rising edge.
4. When Phase Lock is indicated, save the DAC setting (optional). Write 0x04 to location 0x12C.

Note that the EEPROM has limited write cycles (100,000).

Status

To verify the timing status, first write any value to location 0xFC, then check the two bits in the Lock Status nibble located at 0x105 of the Software Time Capture Register. The two bits are:

Bit 5: Input Signal Valid. When set, the GPS receiver time has been validated.

Bit 6: Phase Lock. When set, the output signal timing matches the input signal timing +/-1 microsecond.

If the preset time has been requested, read 0x118. When the 0x04 bit is cleared, the PCI card time has been set to the time in the Preset Time Register. Check location 0x110C in the diagnostic register of the Background Test to determine any errors.

Registers Used in Synchronized Generator mode (1 PPS)

Configuration Register #1:	Location 0x118

Preset Time Register (Seconds-Year):	Locations 0x15B to 0x161
Lock Status:	Location 0x105
Configuration Register #2:	Locations 0x12C and 0x12E
Diagnostic Register:	Location 0x11C

3.4.5 Synchronized Generator – GPS (560-5908)

This mode steers and phase locks the on-board oscillator to the timing provided by a GPS receiver. The PCI card time is automatically set by the time provided by the GPS receiver. The 560-5908 receives transmissions from the NAVSTAR Global Positioning Satellite system and derives time that is traceable to the National Institute of Standards and Technology (NIST). If the GPS receiver indicates that good time is available, the card transfers GPS time into the generator time registers. When the PCI card is within the timing specifications the Locked to GPS flag is set in the Time Register. With satellites visible, the card will normally lock within 10 minutes.

The GPS Module assumes a moderate dynamic environment (LAND mode, velocity <120 knots). The fix mode is AUTO 2-D/3-D and is preferable for most land applications.

Procedure

1. Select GPS mode. Write 0x21 to location 0x118.
2. When Phase Lock is indicated, save the DAC setting (optional). Write 0x04 to location 0x12C.

Note that the EEPROM has limited write cycles (100,000).

Once the GPS Lock is indicated, verify the year. If the reported year is incorrect, use the Preset Time Register (locations 0x160 and 0x161) to set the year. Set the preset time bit by (OR)ing the contents of location 0x118 with a 0x04. Note that the preset year defines the epoch.

Status

Three bits are provided in the Lock Status nibble located at 0x105 of the Software Time Capture Register. The three bits are:

Bit 5: Input Signal Valid. When set, three consecutive PPS signals have been detected where the timing matches.

Bit 6: Phase Lock. When set, the PCI timing matches the GPS signal timing +/1 µs.

Bit 7: GPS Lock. When set, the time includes leap second information and valid position.

Two bits are provided in the Antenna status nibble (location 0xFE) of the Software Time Capture Register indicating antenna operating status.

These are:

Bit 4: Antenna Open. When ‘0’, an antenna is not detected.

Bit 5: Antenna Shorted: When ‘0’, the antenna feedline is shorted.

Satellite Signal Strength is provided at locations 0x198 through 0x1AF. A maximum of six satellites can be tracked, and the information for each satellite is contained in four locations. The first location provides the satellite SV number; the last two locations contain the satellite signal strength.

Prior to reading the satellite data, the satellite update status (location 0x1B0) should be checked. If the location is non-zero, the satellite data should not be read. Following a read of the satellite data, location 0x1B0 should be checked again. If the location is non-zero, the satellite data should be discarded and read again when location 0x1B0 is zero.

Antenna Position is provided at locations 0x108 - 0x11F. Antenna position can be read at any time. However, because updates can occur at any time, it is recommended that the position is read twice and verified. An example of an antenna position is provided, note that all values are BCD except for the direction bytes which are ASCII values indicating the direction.

Registers Used in Synchronized Generator mode (GPS)

Configuration Register #1:	Location 0x118
Preset Time Register (Year):	Locations 0x160 and 0x161
Hardware Status Register:	Location 0xFE
Lock Status Register:	Location 0x105
Diagnostic Register:	Location 0x11C
Antenna Position Register:	Location 0x108 - 0x117
Satellite Signal Strength Register:	Location 0x198 to 0x1AF
Satellite Signal Status Register:	Location 0x1B0

3.4.6 Time Capture

Time information and status are available via the PCI bus in three, 32-bit words. Each word contains packed-BCD time values. The user can capture the time in two different ways. The user may write to an address that latches the time in a set of registers. Alternately, an event (selectable to be external, rate generator, rate synthesizer or time compare) signal will latch the time in a different set of registers permitting time tagging of an event. The event can generate an interrupt to flag its occurrence and the time can then be read over the bus.

Software Time Capture

This feature provides the PCI card’s time at the time of request. The time obtained is the reference time adjusted for any local offset settings (Time Zone). Writing to offset 0xFC will freeze the current time-of-day in the Software Time Registers. They contain packed BCD data, except for the Status bits.

Application

Read the software time to acquire the present time on the card. Note that the PCI card will capture the software time request at the time of arrival. The PCI card has a maximum 150 ns delay after the request before the time is available in the time registers. The PCI card has a Software Time Ready bit in the Hardware Status Register (location 0xFE) that may be used for handshake control for compatibility with existing applications.

Procedure

1. Freeze the time (Software Time Capture) by writing any value to location 0xFC
2. Read the time
3. Read locations 0xFC through 0x107 to obtain the time from 100's of nanoseconds through thousands of years.

Event Time Capture

This feature provides the PCI card's time at the time of the event.

Application

The PCI card will capture the event at the time of arrival. The PCI card has a maximum of 150 ns delay after the event before the time is available in the time registers. The PCI card has an Event bit in the Hardware Status Register (location 0xFE bit 0) that must be used for handshake control.

Procedure

1. Set the Event Time Capture Control register at location 0x12E for the desired event source. The event may be selected to be External, Rate Generator, Rate Synthesizer or Time Compare.
2. Set the edge to be triggered on (rising or falling) using the Event Trigger Edge Control at location 0x12E.
3. Wait for the Event Status bit, or have PCI interrupts enabled. Read location 0xFE, when bit 0 (0x01) is set, the time is ready to read.
4. Read locations 0x174 through 0x17F to obtain the time from 100's of nanoseconds through thousands of years.
5. Clear the Event Status Bit by reading location 0xF8 and ORing it with 0x01.

1.0 Graphical User Interface (GUI)

The GUI TTPCI panel is provided on the CD ROM. This panel is an example program from the SDK software provided. By using the SDK software, a user may further customize the example or create a new one to meet their needs. If the basic interface is sufficient, the SDK software is not used. It is presumed that the customer knows how to create a GUI using the provided SDK software.

1.1 Installation

1.1.1 Procedure

Insert the CD ROM into the CD ROM drive of the computer. Click ***Start>Run and*** select one of the following folders depending on what operating system is on the computer:

Win2knt (Windows 2000 or NT)

Win9x (Windows 95/98)

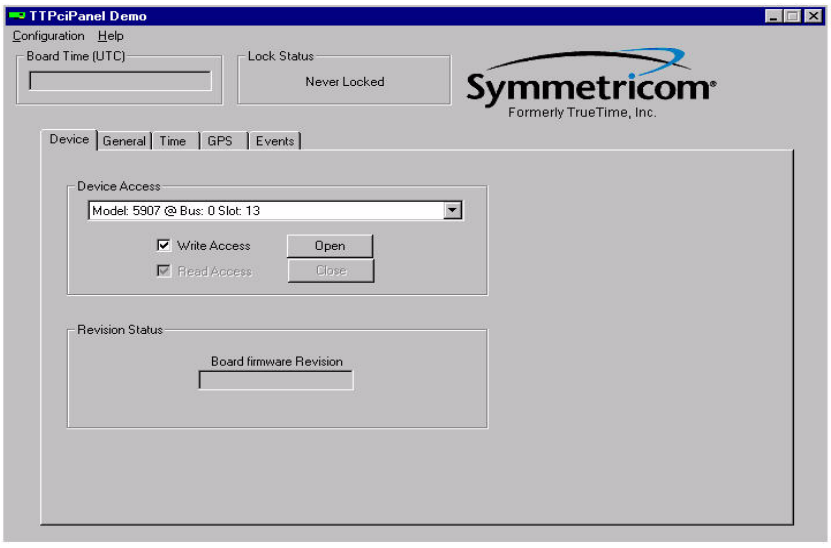
Select "TTPCIPAN.exe" and click on OK. The install Shield will begin running. Follow the instructions on the screen.

To activate the interface, on your desktop, follow these steps:

Start>Programs>TrueTime>TTpciPanel>TTpciPanel

The user interface should appear.

PCI Panel Screen



If you have a 560-5900 or 560-5901 card installed many items under each tab will not be accessible because they do not apply. If a 560-5908 card is installed, all items should be accessible. The 560-5900 or 560-5901 card is not able to translate. The 560-5907 or 560-5908 card can translate. GPS related functions will not be accessible if GPS is not being used.

1.2 PCI Panel Screen Descriptions

1.2.1 Interface Panel

At the top of the panel, the following information is provided:

1. Board Time (UTC) is the current time.
2. Lock Status of the GPS antenna (if used).

   Open = No antenna lock
   OK = Antenna is locked

1.2.2 Device Tab

Device Access

The user should:

1. Use the drop-down menu to select the current device card to be active.
2. Select either Read or Write boxes.
3. Click the ***Open*** button.

By selecting Write, it enables both Read and Write. If you only want to Read, select Read. Once the Open button is clicked on, the user can access the other tabs.

Revision

The current firmware version is shown for informational purposes only. This will not appear if a 560-5900 or 560-5901 card is used.

1.2.3 General Tab

SyncSource

Select the Sync Source using the Sync Source drop down menu.

If you are using a 560-5900 or 560-5901 card, only an input source(Sync) may be selected. Output is always IRIG AM Timecode. If you are using a 560-5907 or 560-5908 card, both an input and output (Output BNC Source) source may be selected.

Phase Compensation

Type a value in the box to specify microseconds.

Output BNC Source

Select the signal to be available at the CODE OUT BNC.

Board Status

These indicators will monitor hardware components of the card as well as the DAC value of the internal oscillator control voltage.

1.2.4 Time Tab

PC Clock Setup

To update, click the box and select minute, hour or day. The Local Time is also shown.

Board Clock

Use the various drop-down menus to select Year, Month, Day, Hour, Minute, or Second.

Leap Second

Click the Leap Second box if the current year is a leap year.

1.2.5 GPS Tab

When the GPS antenna is operational and locked, the following information is provided:

Satellites

PRN, Signal strength, Antenna status and Position.

1.2.6 Events Tab (See 3.3.16 for details)

Events Section

Use the Trigger Source drop-down to select external/internal source.Use the Trigger Edge, Event Time, or Enable Interrupt as needed.

Synthesizer Section

Use the Frequency, or On Time Edge drop-down menu to select from. The Run/Stop button must be in the “Run” position for the synthesizer to be active. Check the Enable Interrupt box to enable the Interrupt.

Rate Generator

In the Rate Generator section, use the Disable drop-down to select from 1 through 10K PPS. Check the Enable Interrupt box to enable the Interrupt.

Time Compare.

Using the various drop-down menus, the user is able to precisely select the time needed for their own purpose. These are self-explanatory. Enable Interrupts as necessary by checking the box.

Index

NOTE: Letters U through Z not used. Numbers refer to sections not page numbers.